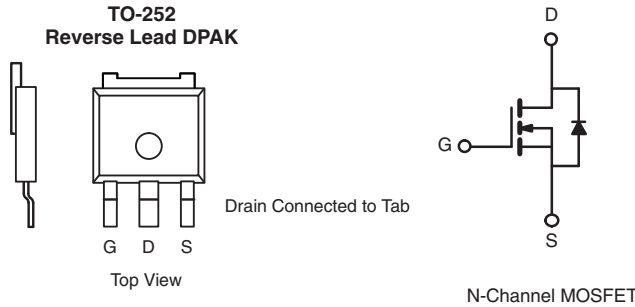


PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0076
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.009
$I_D$ (A)	50
Configuration	Single



### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $R_g$  and UIS Tested
- AEC-Q101 Qualified<sup>d</sup>



ORDERING INFORMATION	
Package	TO-252 Reverse Lead DPAK
Lead (Pb)-free and Halogen-free	SQR50N06-07L-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	$V_{DS}$	60	V		
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current <sup>a</sup>	$I_D$	$T_C = 25$ °C	50	A	
		$T_C = 125$ °C	50		
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	50			
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	200			
Single Pulse Avalanche Current	$I_{AS}$	L = 0.1 mH	48	mJ	
Single Pulse Avalanche Energy			$E_{AS}$		115
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	136	W	
		$T_C = 125$ °C	45		
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	$R_{thJA}$	50	°C/W	
Junction-to-Case (Drain)				

### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

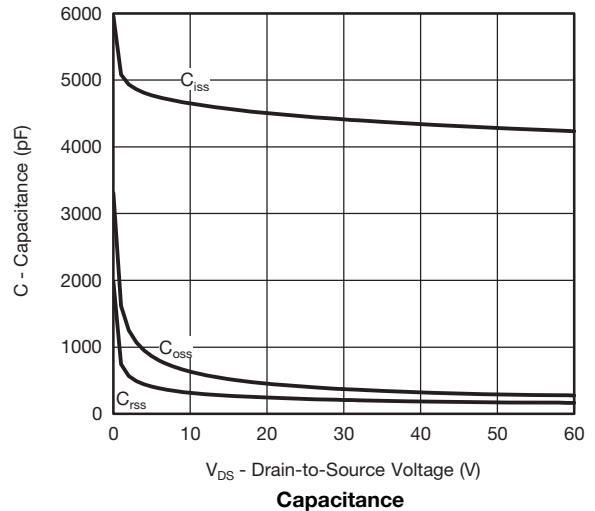
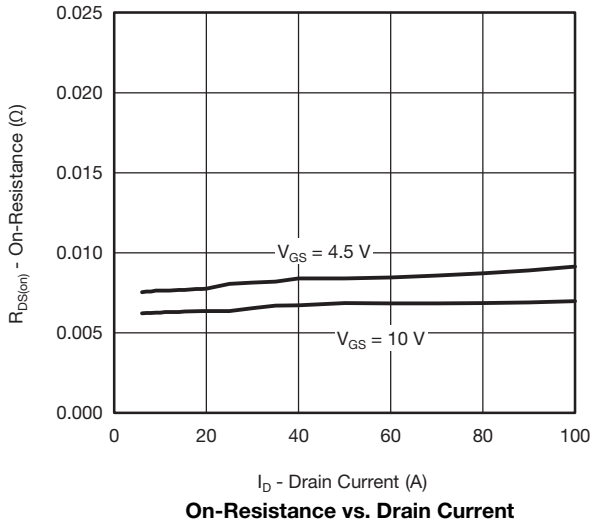
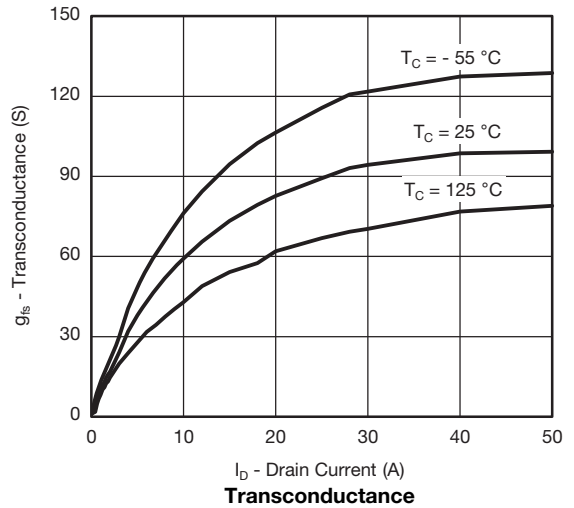
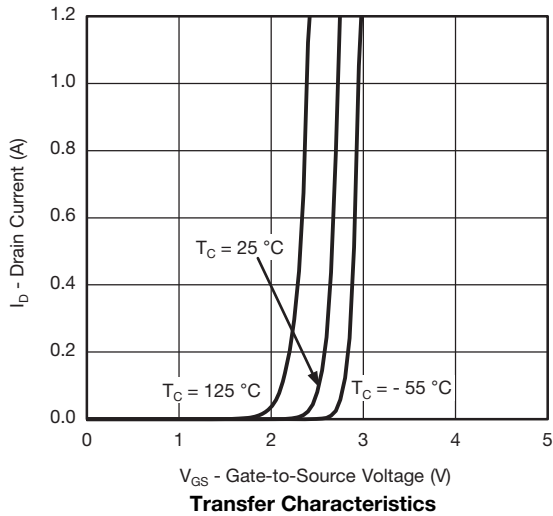
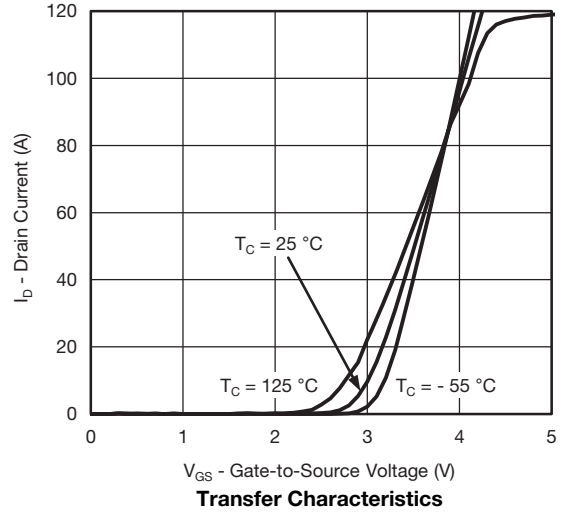
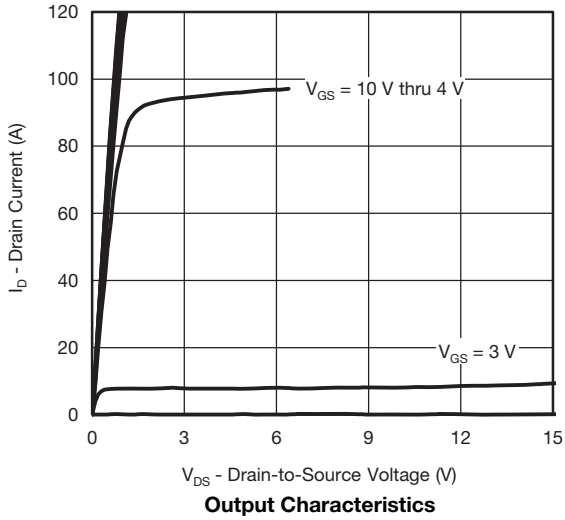
<b>SPECIFICATIONS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.5	2.0	2.5	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$	-	-	1.0	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	50	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	-	0.0064	0.0076	$\Omega$
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0130	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0160	
		$V_{GS} = 4.5\text{ V}$	$I_D = 20\text{ A}$	-	0.0078	0.0090	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		-	82	-	S
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	4455	5570	$\text{pF}$
Output Capacitance	$C_{oss}$			-	407	510	
Reverse Transfer Capacitance	$C_{rss}$			-	223	280	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 30\text{ V}, I_D = 50\text{ A}$	-	80	120	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	11.1	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	15.7	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		1	2	3	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D = 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	12	18	ns
Rise Time <sup>c</sup>	$t_r$			-	13	20	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			-	42	63	
Fall Time <sup>c</sup>	$t_f$			-	7	11	
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>							
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	200	A
Forward Voltage	$V_{SD}$	$I_F = 20\text{ A}, V_{GS} = 0\text{ V}$		-	0.85	1.5	V

**Notes**

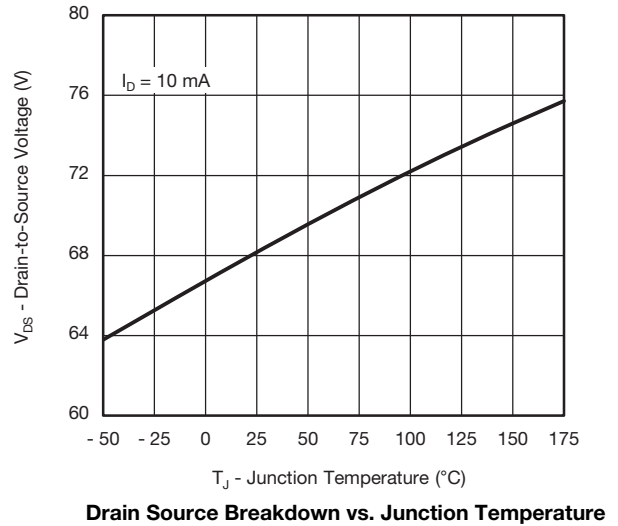
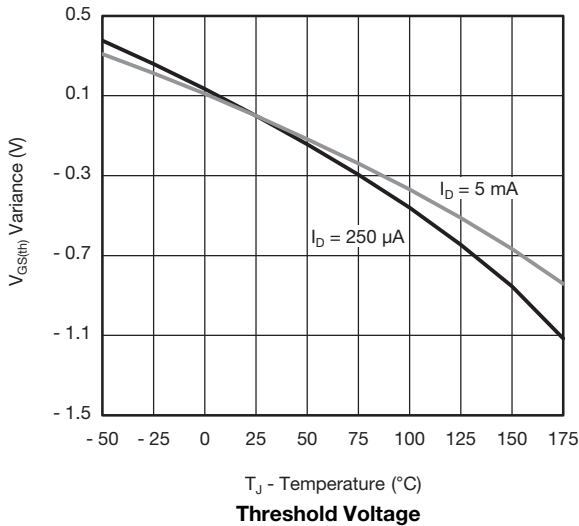
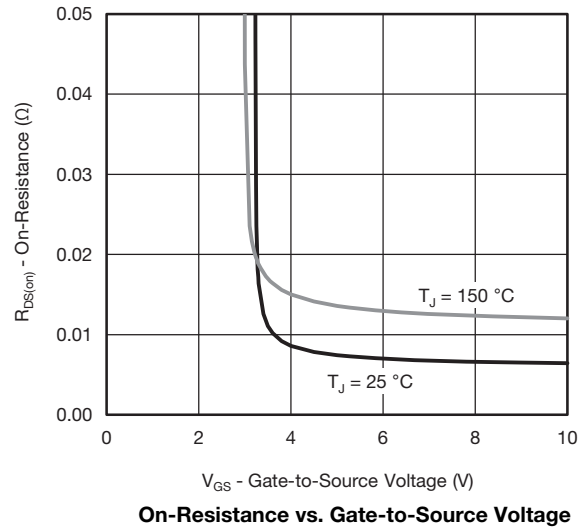
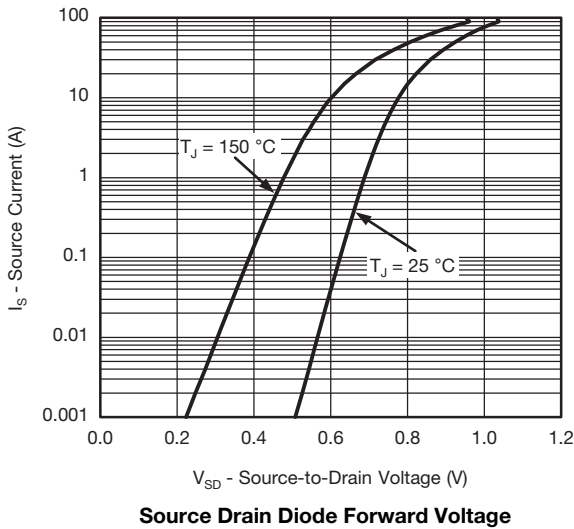
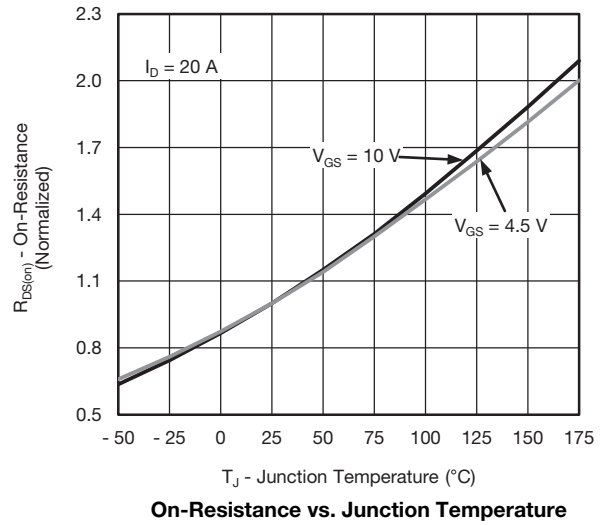
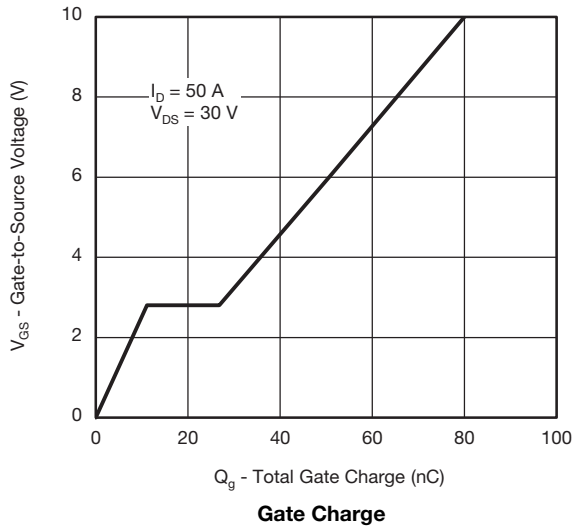
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

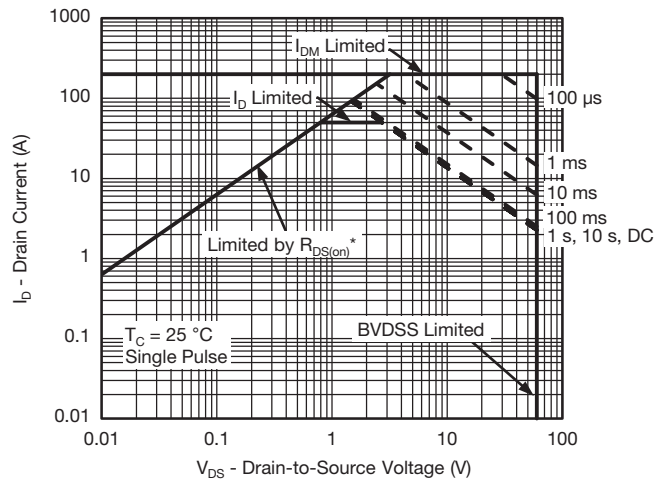
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



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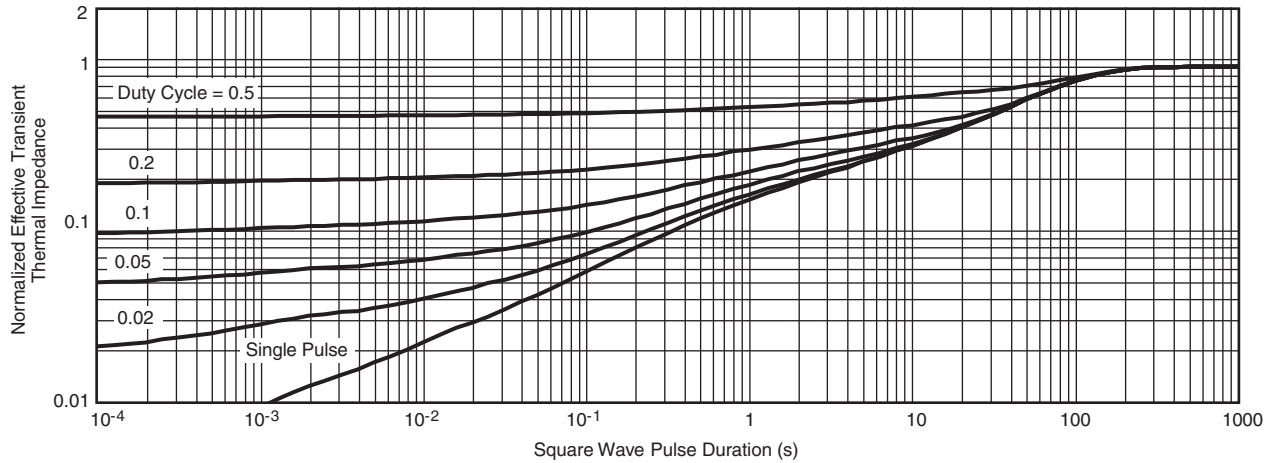


**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



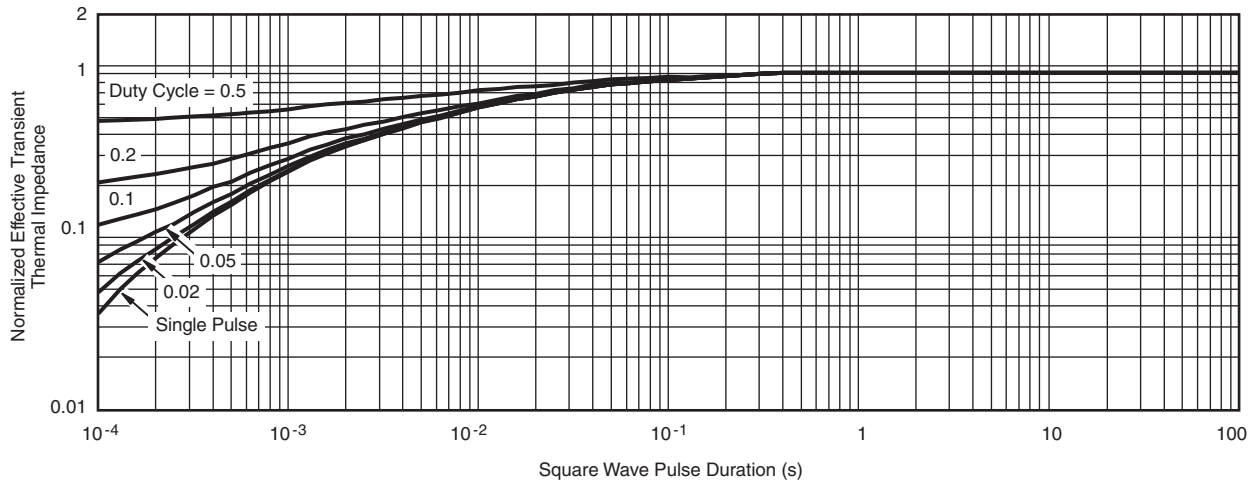
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**THERMAL RATINGS** ( $T_A = 25\text{ °C}$ , unless otherwise noted)

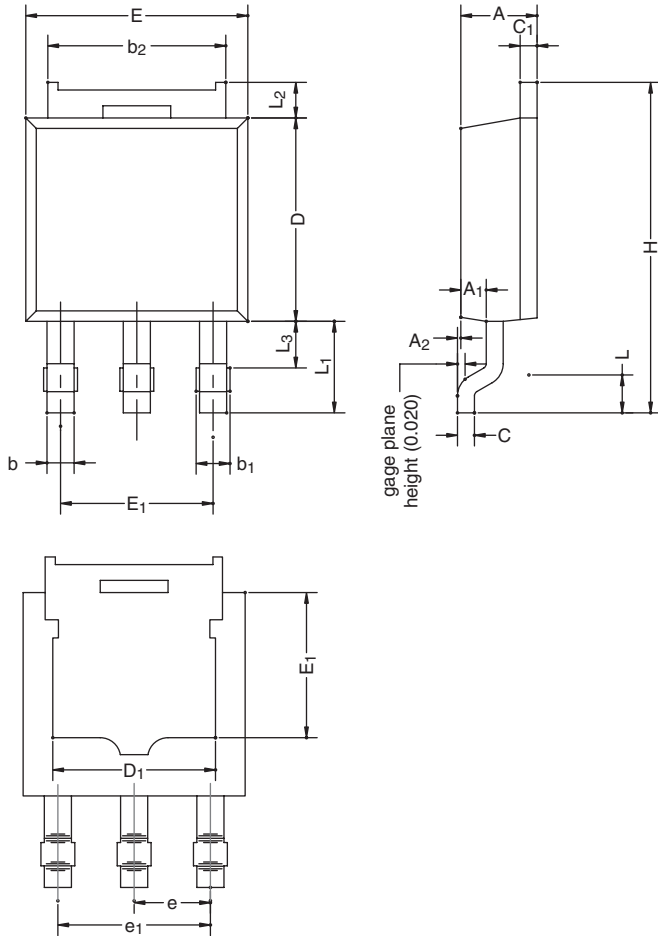


**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ °C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ °C}$ )
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

**TO-252 REVERSE LEAD CASE OUTLINE**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.23	2.33	0.088	0.092
A <sub>1</sub>	0.64	0.89	0.025	0.035
A <sub>2</sub>	0.03	0.23	0.001	0.009
b	0.71	0.88	0.028	0.035
b <sub>1</sub>	0.76	1.14	0.030	0.045
b <sub>2</sub>	5.23	5.44	0.206	0.214
C	0.46	0.58	0.018	0.023
C <sub>1</sub>	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D <sub>1</sub>	4.49	5.00	0.177	0.197
E	6.48	6.73	0.255	0.265
E <sub>1</sub>	4.32	-	0.170	-
e	2.28 BSC		0.090 BSC	
e <sub>1</sub>	4.57 BSC		0.180 BSC	
H	9.65	10.41	0.380	0.410
L	1.40	1.78	0.055	0.070
L <sub>1</sub>	2.74 BSC		0.108 BSC	
L <sub>2</sub>	0.89	1.27	0.035	0.050
L <sub>3</sub>	1.15	1.52	0.040	0.060

ECN: T-08706-Rev. B, 29-Sep-08  
DWG: 5894

**Note**  
Dimension L<sub>3</sub> for reference only.

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